#10

PTO/SB/64 (10-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)	Docket Number (Optional) BTSPH098014

First named inventor: Rolf Grzibek

Application No.: 09/257,638 Group Art Unit: 2614

Filed: February 25, 1999 Examiner: Jean W. Désir

Title: Arrangement for processing video signals

Attention: Office of Petitions
Assistant Commissioner for Patents
Box DAC
Washington, D.C. 20231

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (703)305-9282.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the Office notice or action plus any extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION

NOTE: A grantable petition requires the following items:
(1) Petition fee;
(2) Reply and/or issue fee;
(3) Terminal disclaimer with disclaimer fee -- required for all utility and plant applications filed before June 8, 1995; and for all design applications; and
(4) Statement that the entire delay was unintentional.

1. Petition fee

☐ Small entity - fee $_____ (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☒ Other than small entity - fee $1280 (37 CFR 1.17(m))

2. Reply and/or fee

A. The reply and/or fee to the above-noted Office action in the form of response to Office Action (identify type of reply):

☐ has been filed previously on _____ .
X is enclosed herewith.

B. The issue fee of $ _____

☐ has been paid previously on _____ .
☐ is enclosed herewith.

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3. Terminal disclaimer with disclaimer fee

☐ Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.

☐ A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of $_____ for a small entity or $_____ for other than a small entity) disclaiming a period equivalent to the period of abandonment is enclosed herewith (see PTO/SB/63).

4. Statement. The entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE: The United States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c)(III)(C) and (D))].

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

May 6 2002
Date

Francis A. Davenport
Signature

Telephone Number: 609-734-8964

Francis A. Davenport
Typed or printed name

Thomson multimedia Licensing.

2 Independence Way, Princeton NJ 08540
Address

Enclosures: X Fee Payment

X Reply

☐ Terminal Disclaimer Form

☐ Additional sheets containing statements establishing unintentional delay

☐ ____

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(A)]

I hereby certify that this correspondence is being:

☐ deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Box DAC, Washington, D.C. 20231.

X transmitted by facsimile on the date shown below to the Patent and Trademark Office at (703) 308-6916.

May 6 2002
Date

Francis A. Davenport
Signature

Francis A. Davenport
Typed or printed name of person signing certificate

THOMSON MULTIMEDIA LICENSING INC.

FACSIMILE TRANSMISSION

Thomson Multimedia Licensing Inc.
2 Independence Way
Princeton, NJ 08540

FAX: (609) 734-9700

PHONE: (609) 734-9400

TO: Jean C. Desir (Group Art 2614)

LOCATION: U.S.P.T.O - Washington

FAX NO.: 703-308-6916 **EXT:**

FROM: Francis A. Davenport

609-734-
EXT: 9804 **NO. OF PAGES (including cover)** 13

DATE: Friday 6, 2002

REMARKS: Attached is Petition to Revive for Docket BTSPH0980014 Serial # 09/257,638 filed February 25, 1999

IF YOU ARE MISSING PAGES OR IF NOT RECEIVED PROPERLY,

PLEASE CALL.

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MAY 0 6 2002

PATENT & TRADEMARK OFFICE

PTO/SB/17 (10-01)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) $1280.00

Complete If Known	
Application Number	09/257,638
Filing Date	February 25, 1999
First Named Inventor	Rolf Grzibek
Examiner Name	Jear W. Désir
Group / Art Unit	2614
Attorney Docket No.	BTSPH098014

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 07-0832

Deposit Account Name: THOMSON multimedia Licensing Inc.

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ Payment Enclosed:

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($)000

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	=	Fee Paid
Total Claims		-20 **	3	X	18	=	00
Independent Claims		-3 **	1	X	84	=	00
Multiple Dependent				X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 000

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	1280
141	1,280	241	640	Petition to revive – unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17 (q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
148	740	248	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 1280

SUBMITTED BY				Complete (if applicable)	
Name (Print/Type)	Francis A. Davenport	Registration No. Attorney/Agent)	36,316	Telephone	609-734-9864
Signature	Francis A. Davenport			Date	May 5, 2002

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Rolf Grzibek

Serial No. : 09/257,638

Filed : February 25, 1999

For : PROCESSING INTERLACED AND PSEUDO INTERLACED SIGNALS (as amended)

Art Unit : 2614

Examiner : Jean W. Désir

AMENDMENT PURSUANT TO 37 C. F. R. 1.111

Hon. Assistant Commissioner for Patents

Washington, DC. 20231

Sir:

In response to the Office Action dated October 22, 2001, paper number 7, in the subject patent application, the following amendments are respectfully submitted to place the claims in condition for allowance.

IN THE DRAWINGS:

The Examiner's authorization is requested for changes to FIGURES 1 and 2 shown in red on the separate accompanying sheet.

IN THE SPECIFICATION:

Page 1 line 1, Insert as title

--PROCESSING INTERLACED AND PSEUDO INTERLACED SIGNALS--

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the Hon. Commissioner of Patents and Trademarks, Washington, D. C. 20231 *(Fax. No. 703-3082-6916)* on the date indicated below.

Date Transmitted by Facsimile Monday, May 06, 2002. By:- Francis A. Davenport

Francis A. Davenport,
Reg. No. 36,316

IN THE CLAIMS

Add the following,

--9. A video processor for processing interlaced video signals generated in the interlaced scanning mode, in which two fields constitute one frame, and a pseudo interlaced video signals derived from non-interlaced video signals obtained by means of progressive scanning, said processor comprising:

a video signal processing unit receiving one of an interlaced video signal and a pseudo-interlaced video signal for processing in accordance with control data;

a control unit generating said control data for said processing unit; and,

a clock generator coupled to said control unit for controlling said control data,

wherein said control data initiates processing of said interlaced video signal by said video signal processing unit from the start of the next field, and initiates processing of said pseudo interlaced video signal from the start of the next frame.--

REMARKS

New claim 9 is added. The title is amended to be more descriptive, as required by the Examiner.

FIGURES 1 and 2 are amended to show functional elements as required by the Examiner. Authorization is requested for the changes shown in red on the separate drawing sheet. Withdrawal of the Examiner's objection is respectfully requested.

Claims 1- 8 stand rejected under 35 USC 102(b) as being anticipated by Bhatt (5,610,661).

Applicant traverses this rejection.

In claim 1 applicant recites a video processor for processing interlaced signals or pseudo interlaced signals derived from a progressively scanned source. The processing performed by the video processor depends upon control data generated by a control unit. A clock generator controls the control unit and the video processor. Processing of interlaced signals is controlled such that new control data is taken into account from the start of the next field. Processing of pseudo interlaced signals is

controlled such that new control data is taken into account from the start of the next frame.

In a video processor operable with interlaced signals, applicant recognizes that although progressively scanned signals can be converted into pseudo-interlaced signals to facilitate video processing, the two fields of the pseudo-interlaced contain image detail from the same temporal event. This represents a significant difference from interlaced fields generated by an interlaced source which contain image detail from different temporal events. Applicant further recognizes that to prevent noticeable interference resulting during video processing, for example during a mixing process, processing of pseudo-interlaced signals must be initiated at a time which includes fields from the same temporal event. Thus processing is controlled to occur at the start of a new frame of pseudo-interlaced signal. However, when processing truly interlaced signals, processing is controlled to occur at the start of a new field.

Bhatt teaches an adaptive scan format converter in a system where a received scanning format is automatically converted to a desired display format. For example, a received interlaced signal is automatically converted to progressive format to be compatible with a progressive scan display. Similarly a progressive signal will be passed to the display device without format conversion. Automatic scan conversion is performed seamlessly so that, for example, the conversion between progressive main television program material and interlaced commercial material is produced without artifacts and is essentially invisible to a viewer.

The problem solved by Bhatt is one of providing automatic scan conversion between progressive and interlaced material, with the conversion accomplished seamlessly and essentially invisible to a viewer.

Unlike the teaching of Bhatt, applicant's video processing arrangement is not concerned with scan format conversion. Applicant's inventive arrangement is directed to the video processing of interlaced and pseudo-interlaced signals.

Applicant's claim 1 is not anticipated because Bhatt makes no mention of pseudo-interlaced signals as asserted by the Examiner. Specifically the Examiner asserts that,

> "pseudo-interlaced video signals are derived from non-interlaced video signals obtained by means of progressive scanning (see Fig. 2, Fig. 1 items 14, 36 which disclosed this arrangement)".

The Examiner continues asserting that,

> "at least one video signal-processing unit (see Fig. 2, Fig. 1 items 14, 36) is provided which receives at least an interlaced video signal or at least a pseudo-interlaced video signal".

The Examiner cites items 14, 36 of Bhatt as both the source of pseudo-interlaced video signals, and as a video signal-processing unit. With regard to items 14, 36 Bhatt makes no disclosures such as those asserted by the Examiner. The Examiner's citation of Fig. 2 reveals a detailed schematic of scan format converters as depicted by blocks 14 and 36 of Fig 1, however, in neither Figure 1 nor Figure 2 does Bhatt show or mention pseudo-interlaced signals.

The Examiner continues further asserting that blocks 14 and 36 of Bhatt process the video signals in accordance with "control data generated by control unit (see Fig. 4 item 95)", and "clock generator (see item 70 of Fig. 2)" which controls the control unit (see item 95 of Fig. 4) and/or the video signal-processing unit (see Fig. 2).

The specification of Bhatt discloses that Fig. 1 is a system, comprising a transmitter section blocks 10 - 20 and a receiver section blocks 30 - 39, which are commected via a transmission channel 25. However, Bhatt makes no disclosure of the Examiner's asserted connectivity and control of the video signal-processing unit,

> "in such a way that, when processing an interlaced video signal or a pseudo-interlaced video signal, possibly new control data are generated and/or taken into account as from the start of its next field or its next frame, respectively".

Although Bhatt shows and discloses logic and state machine 95 and sync and mode control network 70, Bhatt makes no mention nor suggestion of operation as the Examiner's asserts. The combination of Bhatt's elements 14 and 36 controlled by items 70 and 95 fail to show or disclose applicant's different timing of new control data as recited in claim 1, wherein, the video signal processing unit is controlled,

> "in such a way that, when processing an interlaced video signal or a pseudo-interlaced video signal, possibly new control data

are generated and/or taken into account as from the start of its next field or its next frame, respectively.

Bhatt makes no mention nor suggestion of any difference in the application of control data between interlaced and pseudo-interlaced signals. Furthermore, Bhatt teaches the use of a frame delay in MUX 80 (Col. 5, line 49) which is disclosed as allowing input switching to occur randomly. Since Bhatt has no reason, nor mechanism to control video signal processing differently between interlaced and pseudo-interlaced signals. Applicant's claim 1 is not anticipated nor rendered obvious by Bhatt and withdrawal of the rejection under 35 USC 102(b) is respectfully requested.

Claim 2 depends from claim 1 and is additionally patentable over Bhatt because applicant recites a buffer memory that is provided for control data. The clock generator controls the buffer memory in such a way that the video signal processing unit takes over new control data at the start of its next field when processing an interlaced video signal or at the start of its next frame when processing a pseudo-interlaced video signal.

The Examiner asserts that elements 82, 84, 86 in Fig 4 of Bhatt provide applicant's recited buffer memory for control data. This assertion is incorrect as Bhatt discloses at Col. 7, from line 18, the use of delays for various video signals. In addition Fig 4 is annotated to show that elements 82, 84, 86 provide delays for video signals I, I or P and P respectively and not control data. Thus Bhatt fails to provide applicant's claim 2 control data delay as the Examiner asserts.

With regard to applicant's claim 3 the Examiner asserts that "clock generator" 70 of Fig. 2, controls "control unit" 95 of Fig. 4, as applicant recites in claim 3. Bhatt discloses coupling between elements 70 of Fig. 2 element 95 of Fig. 4 but provides no teaching or suggestion of asserting new control data at different times depending on the signal being interlaced and pseudo-interlaced. Thus applicant's claim 3 is additionally patentable over the teaching of Bhatt.

In claim 5 applicant recites that the video processor mixes at least two video signals. The Examiner asserts that Bhatt discloses applicant's claim 5 mixing of at least two video signals at column 5 lines 6 - 10. This assertion is without basis in the teaching of Bhatt at column 5 lines 6 - 10 which discloses the operation of de-

interlacer 50 and the creation of a progressive frame from stored odd and even lines. Thus applicant's claim 5 is additionally patentable because Bhatt shows the selection of a single signal source by MUX 46/80, and in addition makes no mention nor suggestion of mixing together two video signals.

Applicant's claims 2 - 8 depend from claim 1 and are, for the same reasons, not anticipated nor rendered obvious by Bhatt. Claims 2, 3 and 5 are additionally patentable over Bhatt for the reasons discussed above.

Newly added claim 9 is directed to applicant's Fig. 2 embodiment. Claim 9 recites a video processor for processing interlaced video signals generated in the interlaced scanning mode, in which two fields constitute one frame, and pseudo interlaced video signals derived from non-interlaced video signals obtained by means of progressive scanning. The processor comprises a video signal processing unit which receives one of an interlaced video signal and a pseudo-interlaced video signal for processing in accordance with control data. A control unit generates the control data for the processing unit and a clock generator is coupled to the control unit for controlling the control data. The control data initiates processing of the interlaced video signal by the video signal processing unit from the start of the next field, and initiates processing of the pseudo interlaced video signal from the start of the next frame.

As discused previously, Bhatt is directed to automatic scan conversion between progressive and interlaced material, with the objective that it is accomplished seamlessly.

Unlike the automatic scan conversion of Bhatt, applicant recognizes that although progressively scanned signals can be converted into pseudo-interlaced signals to facilitate video processing, the two fields of the pseudo-interlaced contain image detail from the same temporal event. This represents a difference from interlaced fields generated by an interlaced source which contain image detail from successive temporal events. Thus applicant's claim 9 ensures that processing of interlaced and pseudo-interlaced fields is initiated at different times depending on the origin of the signal source. As discussed for claim 1 Bhatt, fails to mention or suggest the temporal differences between interlaced and pseudo-interlaced fields

and need to avoid image interference by the use of different control data timing for each interlaced signal type.

Since Bhatt is directed to automatic scan conversion between progressive and interlaced material and makes no mention of temporal content differences between interlaced and pseudo-interlaced fields, applicant's new claim 9 is patentable over Bhatt and the prior art of record.

Applicant has demonstrated that the teachings of Bhatt fail to identify the problem solved by applicant in claims 1 - 8 and newly added claim 9. Applicant respectfully requests the withdrawal of the rejection of claims 1 - 8 and their allowance together with the allowance of claim 9

Respectfully submitted

Rolf Grzibek

5/6/2002

By: Francis A. Davenport

Francis A. Davenport
Reg. No. 36,316
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Patent Operations,
Thomson Multimedia Licensing, Inc.
PO. Box 5312,
Princeton,
NJ 08543-0028

AMENDMENT WITH MARKINGS TO SHOW CHANGES MADE

Page 1 line 1, delete title,

[Arrangement for processing video signals].

and replace with,

--PROCESSING INTERLACED AND PSEUDO INTERLACED SIGNALS--

1/1

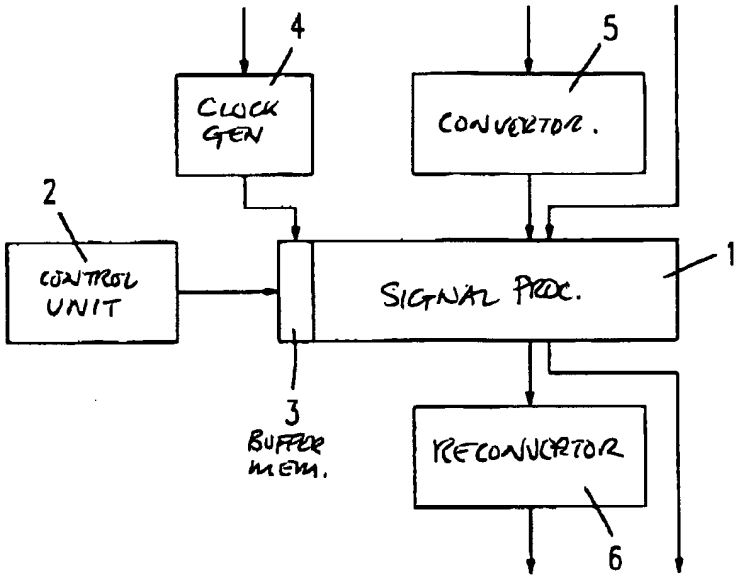
4
5
CLOCK GEN
CONVERTOR.
2
CONTROL UNIT
SIGNAL PROC.
1
3
BUFFER MEM.
RECONVERTOR
6

Fig.1

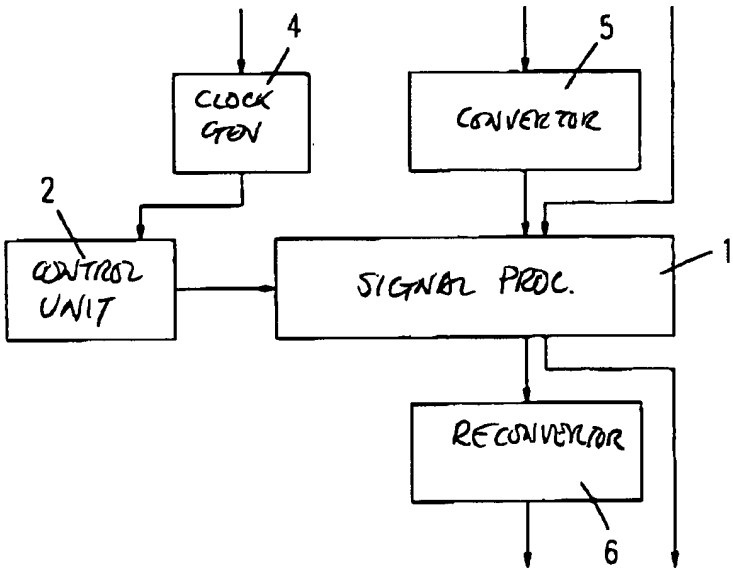
4
5
CLOCK GEN
CONVERTOR
2
CONTROL UNIT
SIGNAL PROC.
1
RECONVERTOR
6

Fig.2